

• General Description

It combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$.

• Features

- AEC-Q101 Qualified
- Low $R_{DS(ON)}$ to minimize conductive loss
- Low Gate Charge for fast switching
- Low Thermal resistance

• Application

- BLDC Motor driver
- DC-DC
- Battery protection

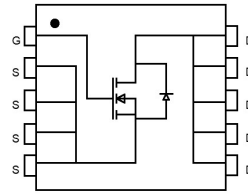
• Ordering Information:

Part NO.	ZMSA006N04HTNC
Marking	06N04H
Packing Information	REEL TAPE
Basic ordering unit (pcs)	2500

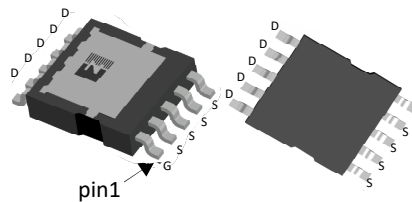
• Absolute Maximum Ratings ($T_C=25^\circ\text{C}$)

Parameter	Symbol	Conditions	Value	Unit
Drain-Source Voltage	V_{DS}		40	V
Gate-Source Voltage ^①	V_{GS}		± 20	V
Continuous Drain Current	I_D	$T_C=25^\circ\text{C}$	340	A
	I_D	$T_C=75^\circ\text{C}$	280	A
	I_D	$T_C=100^\circ\text{C}$	242	A
Pulsed Drain Current	I_{DM}	Pulsed; $t_p \leq 10 \mu\text{s}$; $T_{mb} = 25^\circ\text{C}$;	1020	A
Total Power Dissipation	P_D	$T_C=25^\circ\text{C}$	200	W
Total Power Dissipation	P_D	$T_A=25^\circ\text{C}$	5.0	W
Operating Junction Temperature	T_J		-55 to +175	$^\circ\text{C}$
Storage Temperature	T_{STG}		-55 to +175	$^\circ\text{C}$
Single Pulse Avalanche Energy	E_{AS}	$L=0.1\text{mH}$, $V_{GS}=10\text{V}$, $R_g=25\Omega$,	360	mJ
		$L=0.5\text{mH}$, $V_{GS}=10\text{V}$, $R_g=25\Omega$,	680	mJ
ESD Level (HBM)	CLASS 2			

• Product Summary



$V_{DS} = 40\text{V}$
 $R_{DS(ON)} = 0.6\text{m}\Omega$
 $I_D = 340\text{A}$



TCPAK5x7



•Thermal resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case	R_{thJC}		-	0.75	°C/W
Thermal resistance, junction-ambient	$R_{thJA}^{②}$		-	30	°C/W
Soldering temperature	T_{sold}		-	260	°C

•Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	40			V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	2	2.7	4	V
Drain-Source Leakage Current	I_{DSS}	$V_{GS} = 0V, V_{DS} = 40V$			1.0	μA
Gate- Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20V, V_{DS} = 0V$			100	nA
Static Drain-source On Resistance	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 40A$		0.6	0.74	m Ω
Forward Transconductance	g_{FS}	$V_{DS} = 5V, I_{SD} = 10A$		30		S
Diode Forward Voltage	V_{FSD}	$V_{GS} = 0V, I_{SD} = 40A$			1.3	V

•Dynamic characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	C_{iss}	$f = 1MHz, V_{DS} = 25V$	-	6900	-	pF
Output capacitance	C_{oss}		-	2100	-	
Reverse transfer capacitance	C_{rss}		-	86	-	
Gate Resistance	R_g	$f = 1MHz$	-	1.4		Ω
Total gate charge	Q_g	$V_{DD} = 15V, I_D = 20A, V_{GS} = 10V$	-	94	-	nC
Gate - Source charge	Q_{gs}		-	21	-	
Gate - Drain charge	Q_{gd}		-	26	-	
Turn-ON Delay time	$t_{D(on)}$	$V_{GS} = 10V, V_{DS} = 15V, R_G = 3.3\Omega, I_D = 20A$	-	16	-	ns
Turn-ON Rise time	t_r		-	11	-	ns
Turn-Off Delay time	$t_{D(off)}$		-	40	-	ns
Turn-Off Fall time	t_f		-	19	-	ns
Reverse Recovery Time	t_{RR}	$V_{DD} = 20V, di_S/dt = 100A/\mu s, I_S = 50A$	-	72	-	ns
Reverse Recovery Charge	Q_{RR}		-	133	-	nC

Fig.1 Gate-Charge Characteristics

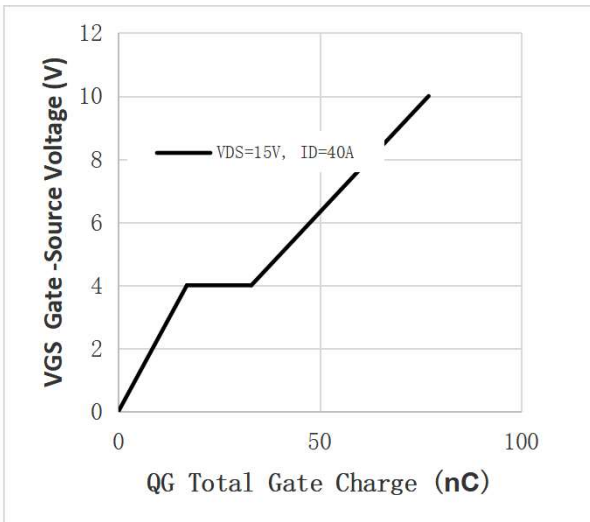


Fig.2 Capacitance Characteristics

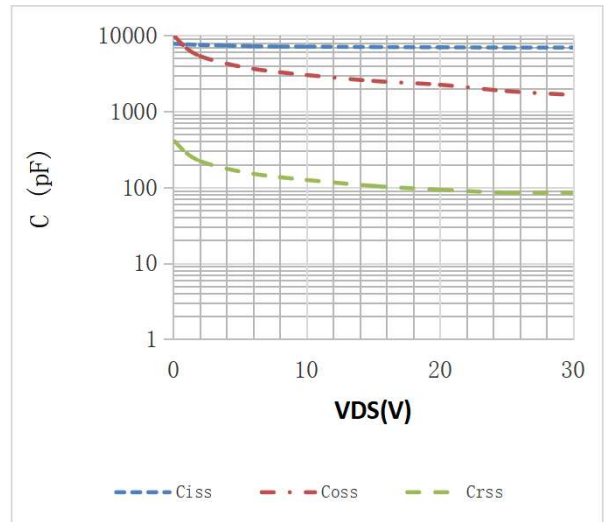


Fig.3 Power Dissipation

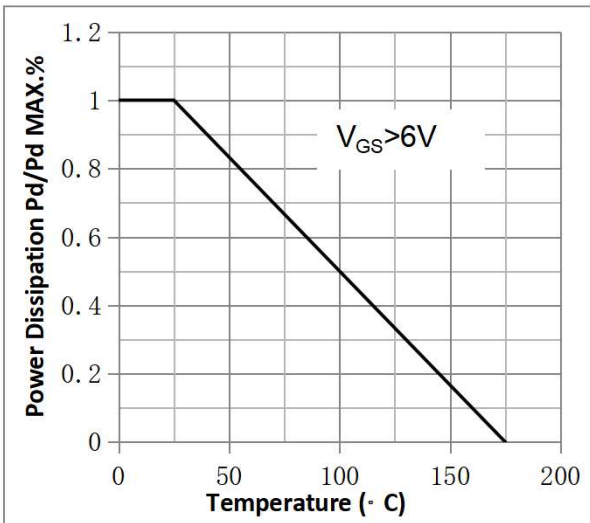


Fig.4 Typical output Characteristics

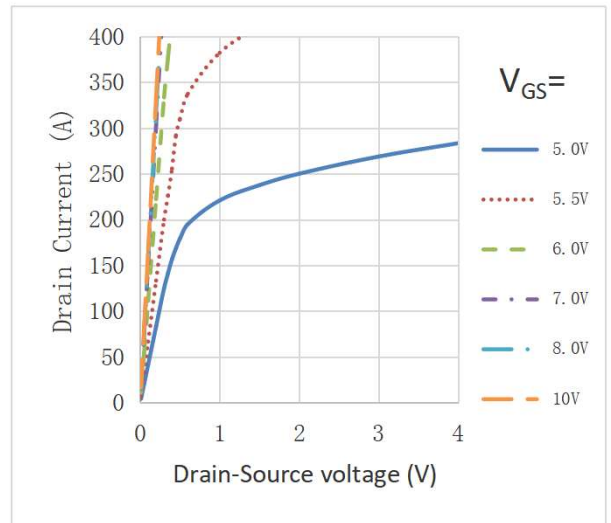


Fig.5 Threshold Voltage V.S Junction Temperature

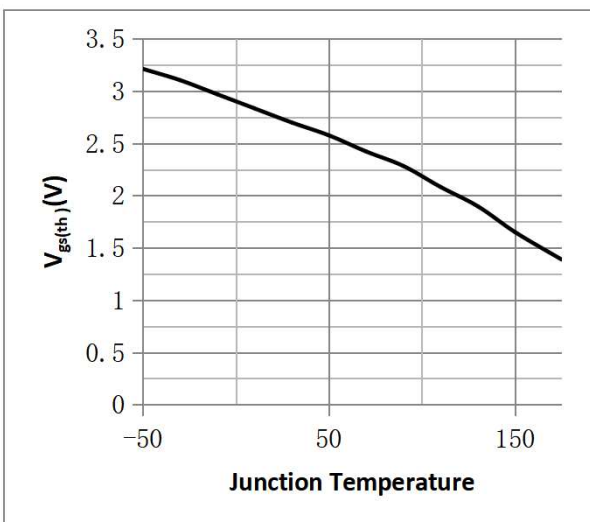


Fig.6 Resistance V.S Drain Current

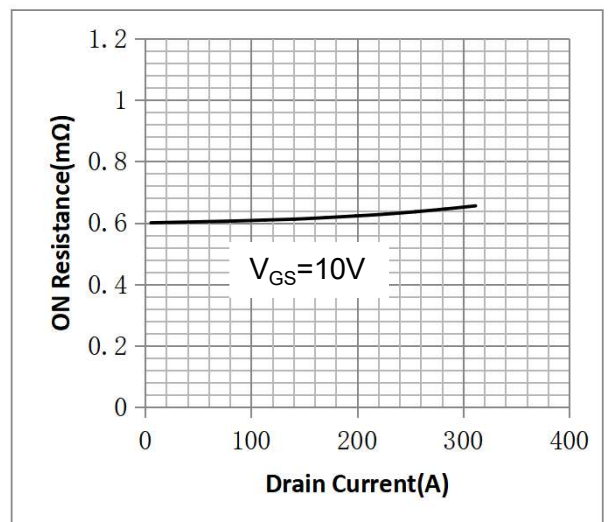


Fig.7 On-Resistance VS Gate Source Voltage

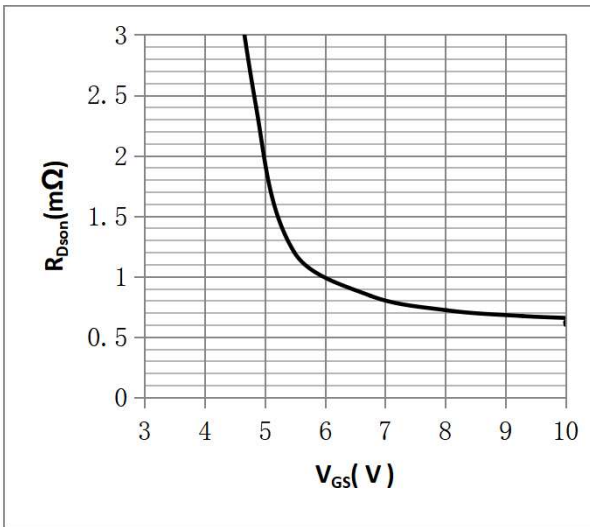


Fig.8 On-Resistance V.S Junction Temperature

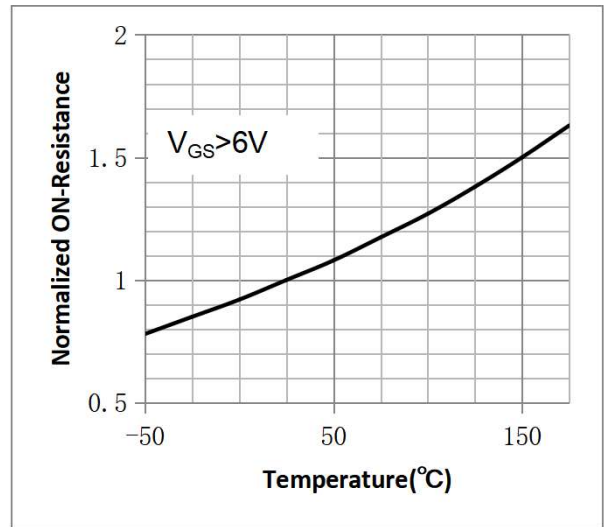


Figure 9. Diode Forward Voltage vs. Current

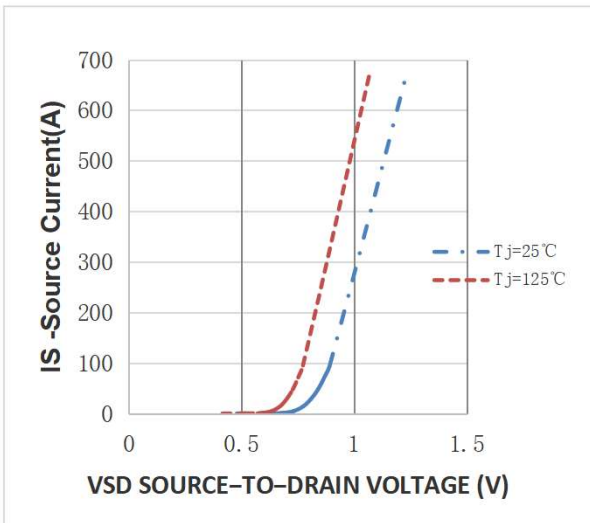


Figure 10. Transfer Characteristics

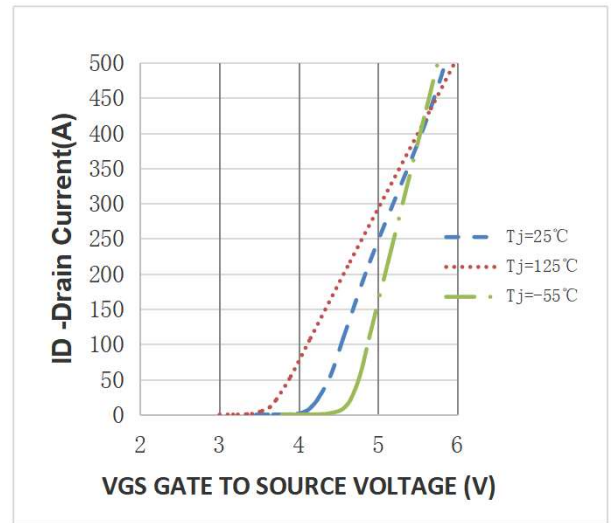


Fig.11 Safe Operating Area

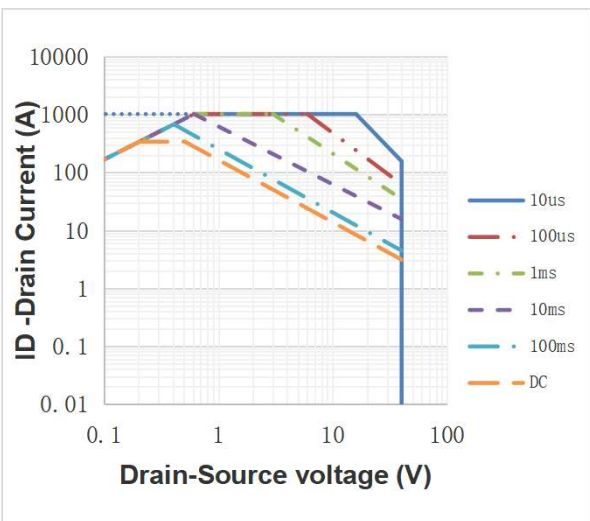
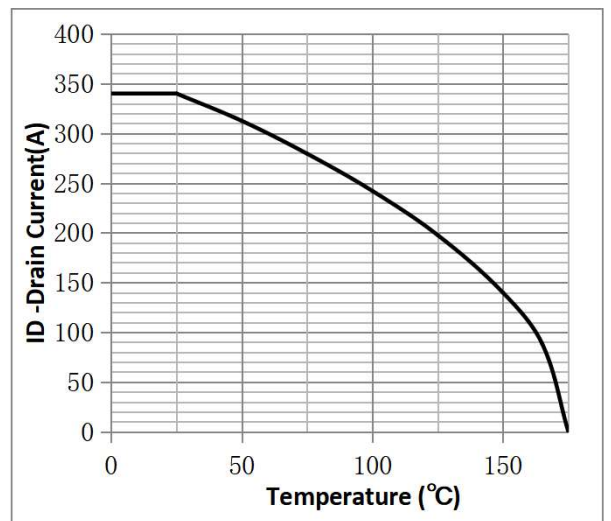
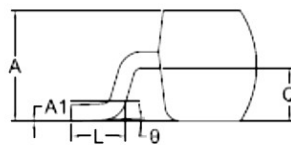
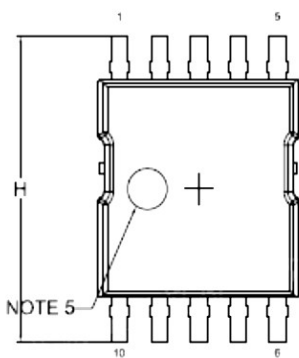
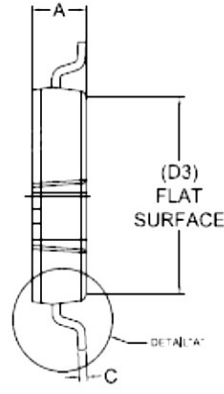
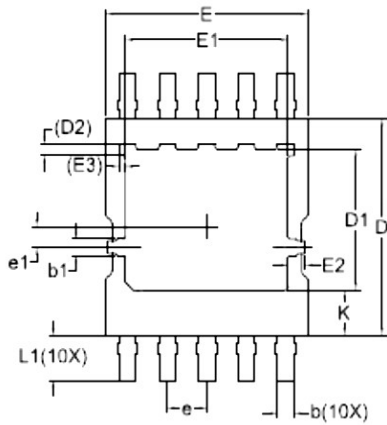


Fig.12 ID vs. Junction Temperature^③



•TCPAK5x7 Package Outline



MILLIMETERS			
DIM	MIN	NOM	MAX
A	1,25	1,35	1,45
A1	-0,05	0	0,075
b	0,36	0,41	0,46
b1	0,30	0,40	0,50
c	0,16	0,20	0,26
D	5,20	5,30	5,40
D1	3,35	3,45	3,55
D2	0,20 REF		
D3	4,82 REF		
E	5,00	5,10	5,20
E1	4,02	4,12	4,22
E2	0,30	0,44	0,50
E3	0,14 REF		
e	1,00 BSC		
e1	0,50 BSC		
K	1,00	1,10	1,20
H	7,30	7,50	7,70
L	0,49	0,69	0,89
L1	0,90	1,10	1,30
Q	0,60	0,65	0,70
θ	0°	2,5°	5°

Note:

- ① Pulse : $V_{GS}=+20V/-20V$, Duty cycle=50%, $T_j=175^{\circ}C$, $t=1000$ hours; For DC , the following test conditions can be passed: $V_{GS}=+20V/-10V$, $T_j=175^{\circ}C$, $t=1000$ hours;
- ② Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate;
- ③ Practically the current will be limited by PCB, thermal design and operating temperature. $V_{GS}=10V$.

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Revision History

Version	Date	Change
A	2023.10.24	new
B	2024.4.16	Modified ciss,Qg,switch time
C	2024.6.19	Modified Package NAME AS TCPAK5×7
D	2024.9.24	Modified Rdson limit 0.8 to 0.74
E	2024.11.27	Modified basic ordering unit.